

Sub B27

D1

a' Sub B37

D1

2. (Amended) The device of Claim 20 wherein each of the dielectric layer, the buffer layer, and the blocking layer comprise epitaxial layers.

3. (Amended) The device of Claim 20 wherein the gate electrode comprises silicon germanium.

4. (Amended) The device of Claim 20 wherein each of the buffer layer and the blocking layer comprise silicon.

5. (Amended) The device of Claim 20 wherein each of the source/drain regions comprises silicon germanium.

6. The device of Claim 5 wherein each of the source/drain regions comprises amorphous silicon germanium.

D1

7. (Amended) The device of Claim 20 wherein the dielectric layer is selected from the group consisting of oxides of zircon, oxides of titanium, oxides of tantalum, and oxides of hafnium.

a²

Sub B4

8. (Amended) The device of Claim 20 wherein the blocking layer comprises less than or equal to ten layers of atomic silicon in thickness.

9. (Amended) The device of Claim 20 wherein the buffer layer comprises less than or equal to ten layers of atomic silicon in thickness.

10. Canceled.

a³ D1

11. (Amended) The device of Claim 21 wherein the gate electrode comprises a metal.

12. (Amended) The device of Claim 21 wherein each of the source/drain regions has a depth into the well of about 100 to about 1000 Angstroms.

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13. (Amended) The device of Claim 21 wherein the source/drain regions comprise amorphous material.

20. (New) A semiconductor device formed on a substrate and comprising:
a well;
a channel region of first conductivity type and being in the well;
a buffer layer overlying the dielectric layer;
a dielectric layer overlying the channel region;
a gate electrode overlying the buffer layer;
a blocking layer overlying the gate electrode; and
two source/drain regions of second conductivity type formed on opposite sides of the channel region.

21. (New) A semiconductor device formed on a substrate and comprising:
a well;
a channel region of first conductivity type and being in the well;
a dielectric layer overlying the channel;
a gate electrode overlying the dielectric layer; and
two source/drain regions of second conductivity type formed on opposite sides of the channel region, wherein the source/drain regions comprise silicon germanium.

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